Transfer Type Bit 4: (Processor Deferred Read)

This bit may be set when the processor initiates a deferred read and is cleared when deferred read data is returned to the processor.

Transfer Type Bit 5: (PCI Deferred Read)

This bit may be set when an initiator requests a PCI deferred read and is cleared when the PCI device returns read data to the matched data buffer.

On page 15, lines 13-26: lines 12-25 KC 7/5/09

Many signals can be used to control communications between the Pentium[[7]]® Pro Processor 41, bridge circuit 40 and PCI device 44. These signals are also used to designate which address (or data) buffer should receive a particular request from the Pentium[[7]]® Pro Processor 41. As can be imagined, it is important for the system to ensure that the proper address is sent to the proper PCI device 44. In addition, because the address and data buffers are separated, the system needs to monitor which address and data buffer has completed its task and is available for more work. The following signals, as listed in Table 3, are used by the internal modules of the bridge circuit 40 to coordinate the movement of information between the modules and by the PCI master controller. Signals that begin with "HS" communicate between the PCI master controller 57 and the CPU slave controller 55. Signals that begin with "HM" communicate between the PCI master controller 57 and the CPU Bus master controller 50. Signals that begin with "PCI" communicate internally between the PCI master controller 57 and a PCI bus interface controller (not shown) which actually controls signals on the PCI bus.

On page 17, lines 9-12 (indents corrected):

The embodiment of the DBA system 60 illustrated in Figure 4 includes an input arbiter 130 that provides control signals to the address buffers 115a-c. The input arbiter 130 interprets the signals described in Table 3, and toggles write enable signals 132a-c that direct the incoming address request 110 into an available buffer.

On page 17, lines 13-19:

As discussed above, the address buffers 115a-c may include three signal paths; one input and two output. The input path may be used to write PCI address transfer requests into the address buffers 115a-c. This may be done when both the HS_REQ and HS_ACK signals are asserted, indicating that the Pentium[[7]]® Pro processor 41 has put